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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
09/718,932	11/22/2000	Mark Pavier	IR-17732-2498	2141

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EXAMINER	
ROMAN, ANGEL	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/718,932	PAVIER, MARK	
	Examiner	Art Unit	
	Angel Roman	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/22/00* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4)☐ Interview Summary (PTO-413) Paper No(s). _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-5, 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phy U.S. Patent 4,688,075.

Phy discloses a process of connecting a semiconductor die to a substrate having a top surface, said process comprising the steps of; providing a thin, flexible, heat curable polyimide film 127 which is of a first area; placing said film on a thin semiconductor wafer of a second area, said semiconductor wafer being provided with a plurality of spaced apart semiconductor die, each of said semiconductor die having a respective third area which is substantially less than said firs area (see figure 4); preheating said semiconductor wafer and said film to partially cured said film, thereby forming adhesion between said thin flexible film and said semiconductor wafer (see column 4, lines 50-55); thereafter simultaneously singulating both said thin flexible film and said plurality of identical semiconductor die to form individual elements (see column 4, lines 45-50); thereafter applying at least one of said singulated semiconductor to the top surface of said substrate surface with the film on said die pressed against said top surface and adhered thereto; and thereafter heating said one semiconductor die to fully

cure said thin flexible film to firmly adhere said die to said substrate (see column 3, lines 39-45). Said first area is substantially identical to, or different from, said second area (see figure 4). The film on said die has the same or different area as that of said die after assembly onto said substrate. Exemplary materials for the substrate include conductors, metals and alloys (see column 3, lines 21-25). Phy also discloses heating an entire assembly of figure 2B (see column 3, lines 39-45).

Phy is applied as above but lacks anticipation on using insulative polyimide in the disclosed embodiment, and heating the substrate prior to placing the singulated semiconductor on the substrate.

With respect to using insulative polyimide instead of conductive polyimide, it is conventional in the art to used insulative polyimide as an adhesive material for adhesive bonding processes, therefore it would have been obvious to one having ordinary skills in the art at the time the invention was made to use insulative polyimide in the primary reference of Phy for the reasons given above. Furthermore using insulative polyimide in the primary reference of Phy is considered to be routine optimization of the embodiments disclosed in Phy, therefore it would have been within the level of one having ordinary skills in the art to perform such modifications and it would have been obvious for a person having ordinary skills in the art at the time the invention was made to use insulating polyimide if insulating properties are desire.

Regarding heating the substrate prior to placing the singulated semiconductor on the substrate, it is well known in the art to perform a bonding process by preheating a substrate to be bonded in the bonding process, therefore it would have been obvious to

one having ordinary skills in the art at the time the invention was made to heat the substrate in the primary reference of Phy. Heating the substrate prior to a bonding step to a semiconductor die is only considered to be routine optimization of the embodiments disclosed by Phy therefore it would have been obvious to one having ordinary skills in the art at the time the invention was made to heat the substrate prior to the bonding step in the primary reference of Phy.

3. Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phy U.S. Patent 4,688,075 in view of Burns U.S. Patent 5,221,642.

Phy is applied as above but lacks anticipation on adhering a second semiconductor die with a second adhesive film thereon to said substrate at a position laterally remove from a first die and disclosing a substrate consisting of a lead frame. Regarding adhering a second semiconductor die with a second adhesive film thereon to a substrate at a position laterally remove from a first die, Burns discloses adhering a second semiconductor die with a second adhesive film thereon to a substrate at a position laterally remove from a first die (see figure 4b). In view of this disclosure it would have been obvious to a person having ordinary skills in the art at the time the invention was made to adhere a second semiconductor die with a second adhesive film thereon to a substrate at a position laterally remove from a first die as disclose in Burns in the primary reference of Phy because it is a conventional form of arranging dies on a substrate in the semiconductor manufacturing industries.

With respect to disclosing a substrate consisting of a lead frame, Burns discloses a substrate consisting of a lead frame (see Abstract). In view of this disclosure it would have been obvious to a person having ordinary skills in the art at the time the invention was made to disclose a substrate consisting of a lead frame as disclose in Burns in the primary reference of Phy because lead frames are conventionally used for semiconductor substrate packaging processes.

4. Claims 7, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phy U.S. Patent 4,688,075 in view of Takiar et al. U.S. Patent 5,442,435.

Phy is applied as above but lacks anticipation on adhering a second die with a second adhesive film thereon to the top of said die secured to said substrate and a process wherein said adhesive film has a smaller area than said top surface of said die and wherein said second die and said second adhesive film both have the same area as said adhesive film.

With respect to adhering a second die with a second adhesive film thereon to a top of a die secured to a substrate Takiar et al. discloses adhering a second die with a second adhesive film thereon to a top of a die secured to a substrate (see figure 3). In view of this disclosure it would have been obvious to a person having ordinary skills in the art at the time the invention was made to adhere a second die with a second adhesive film thereon to a top of a die secured to a substrate as disclose in Takiar et al. in the primary reference of Phy because it is a conventional process of stacking dices in the semiconductor manufacturing industries.

Regarding a process wherein an adhesive film has a smaller area than a top surface of a die and wherein a second die and a second adhesive film both have the same area as said adhesive film. This limitation, is only considered to be an obvious modification of the shape of the area disclosed by Takiar et al. as the courts have held that a change in shape or configuration, without any criticality, is within the level of skill in the art as the particular shape claimed by applicant is nothing more than one of numerous shapes that a person having ordinary skill in the art will find obvious to provide using routine experimentation based on its suitability for the intended use of the invention. See In re Dailey, 149 USPQ 47 (CCPA 1976).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Phy U.S. Patent 4,688,075 in view of the prior art disclose on page 4, line 19 of the specification (hereinafter Prior Art).

Phy is applied as above but lacks anticipation on removing said dice and film to said substrate by a pick and place apparatus.

Prior Art discloses removing a dice and film to said substrate by a conventional pick and place apparatus. In view of this disclosure it would have been obvious to a person having ordinary skills in the art at the time the invention was made to remove a dice and film to said substrate by a pick and place apparatus as disclose in Prior Art in the primary reference of Phy because it is a conventional method of handling a semiconductor device.

Response to Arguments

6. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (703) 306-0207. The examiner can normally be reached on Monday-Friday 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

AR
March 22, 2002